



## Product/Process Change Notice - PCN 15\_0178 Rev. A

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

*Note: Revised fields are indicated by a red field name. See Appendix B for revision history.*

**PCN Title:** ADV7619 Settings and Related Data Sheet Specification updates  
**Publication Date:** 09-Oct-2015  
**Effectivity Date:** 09-Oct-2015 *(the earliest date that a customer could expect to receive changed material)*

### Revision Description:

Update the pixel clock frequency from which the new configuration settings must be applied (170MHz). Update effectivity date code.

### Description Of Change

#### 1. Configuration Setting Change:

The ADV7619 recommended setting scripts for video resolutions with a pixel clock of over 170MHz have been updated to incorporate the following writes:

```
; Added write 98 00 19 ; Set VID_STD  
; Added write 98 01 05 ; Prim_Mode =101b HDMI-Comp  
; Added write 98 DD 00 ; Default value  
; Added write 98 E7 04 ; ADI Required Write
```

The ADV7619 settings are outlined in the ADV7619 Required Settings document and the recommended settings script file available from Engineer Zone.

#### 2. Datasheet Addition:

An additional clock duty cycle specification for video resolutions with a pixel clock of over 170MHz was added to the ADV7619 datasheet.

Specification: LLC Mark-Space Ratio

Time Descriptor: t9:t10

Description: For input video resolutions with a pixel clock frequency > 170 MHz

Minimum Spec: 40:60 % duty cycle

Maximum Spec: 60:40 % duty cycle

The ADV7619 datasheet is available from the ADV7619 product page on the Analog Devices website.

### Reason For Change

In conjunction with the silicon, the ADV7619 recommended I2C settings are a critical element of an overall stable solution. This change is being made to improve the timing-related stability of the I2C settings at certain combinations of material, voltage and temperature.

The modification changes the clock path employed for video resolutions with a pixel clock of over 170MHz. It has been confirmed that the new clock path resolves the timing-related stability issues observed with the old clock path at certain combinations of material, voltage and temperature. The new clock path has a slightly higher level of clock duty cycle distortion, please see the above change description for the clock duty cycle specification.

### Impact of the change (positive or negative) on fit, form, function & reliability

The following are the impacts of this change:

1. Application Software Change

Customers must add the new configuration settings into their application software to guarantee the most robust performance of ADV7619

## 2. Duty Cycle Ratio

Customers must analyse their application hardware to ensure that their setup and hold timing margin is still sufficient given the increased clock duty cycle.

### **Product Identification** *(this section will describe how to identify the changed material)*

This change is effective from date code 1539.

### **Summary of Supporting Information**

The changes described above are reflected in the ADV7619 Rev. D data sheet, the ADV7619 Required Settings document Rev 1.7 and the ADV7619 recommended settings script file Rev 1.8.

**Supporting Documents**      None

**For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.**

<b>Americas:</b>	PCN_Americas@analog.com	<b>Europe:</b>	PCN_Europe@analog.com	<b>Japan:</b>	PCN_Japan@analog.com
				<b>Rest of Asia:</b>	PCN_ROA@analog.com

**Appendix A - Affected ADI Models**

**Existing Parts - Product Family / Model Number (2)**

ADV7619 / ADV7619KSVZ

ADV7619 / ADV7619KSVZ-P

**Appendix B - Revision History**

<b>Rev</b>	<b>Publish Date</b>	<b>Effectivity Date</b>	<b>Rev Description</b>
Rev. -	22-Sep-2015	22-Sep-2015	Initial Release
Rev. A	09-Oct-2015	09-Oct-2015	Update the pixel clock frequency from which the new configuration settings must be applied (170MHz). Update effectivity date code.

Analog Devices, Inc.

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